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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,834	03/04/2004	Peer Gil Schmitt	003921.00148	3853

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,834	SCHMITT, PEER GIL	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-9* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 12/16/2005 has been entered.

2. Claims 1-9 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3,6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Mukai (U.S. Patent No. 6,310,818).

Regarding claim 1, Mukai discloses a memory device (Figure 3), comprising:

a plurality of addressable memory cells (Figure 3, memory cell), each memory cell configured to store a first bit (Figure 4, BLA) and a second bit (BLB), each memory cell (ABSTRACT) including:

a first storage circuit configured to store the first bit (Figure 4, Q4) ; and

a second storage circuit (Figure 4, Q3) configured to store the second bit and coupled to the first storage circuit (Figure 4), and further configured to deactivate the first storage circuit based on the second bit (Column 6, lines 45-52).

Regarding claim 2, Mukai discloses a first bit line (Figure 3, BLA) coupled to at least one of the memory cells (Figure 3, BLA coupled memory cell 31) , wherein the first storage circuit (Figure 4, 31) of the at least one memory cell includes: an enable node (Figure 5, N1, Column 6, lines 6-12) and a first output node (Figure 5, N1, Column 6, lines 6-12) , wherein the first storage circuit has either a high or low impedance at the first output node depending upon a logical value of the enable node (Column 6, lines 64-67, Column 7, lines 1-6), the first bit line selectively receiving a logical value of the first output node, and wherein the second storage circuit of the at least one memory cell (Figure 4, 31) includes: a second output node (Figure 5, N2) configured to control the enable node, the first bit line selectively receiving a logical value of the second output node (Figure 5, N2, BLB, potential value of N2 same as potential value N2, Column 7, lines 8-23), and further including a second bit line (Figure 4, BLB) coupled to the at least one memory cell (Figure 4, 31), wherein the first storage circuit of the at least one memory cell includes a third output node (Figure 4, node between Q3 and 34) , wherein the first storage circuit has either a high or low impedance at the third output node depending upon a logical value of the enable node, the third output node having a logic value opposite (Figure 4, node between Q3 and 34 opposite node N1) the first output node when the first storage circuit has a low impedance at the first and third output nodes, the second bit line selectively receiving a logical value of the third output node, and wherein the second storage circuit of the at least one memory cell includes a fourth output node (Figure 4, node between Q4 and 34) having a value opposite the second output node, the second bit line selectively receiving a logical value of the fourth output

node (Figure 4 has four nodes N1, inputs of 33, N2 outputs of 33, N3 inputs of 34, N4 outputs of 34).

Regarding claims 6-9, Mukai discloses an apparatus, comprising: a plurality of dual-bit memory cells (Figure 3) , each memory cell (Figure 4) including:

a first storage circuit configured to store a first bit (Figure 4, 33) , and a second storage circuit (figure 4, 34) configured to store a second bit (ABSTRACT); a first plurality of word lines Figure 4, WLA) each controlling one of the first storage circuits; and a second plurality of word lines (Figure 4, WLB) each controlling one of the second storage circuits, wherein the first storage circuit includes a transistor having a gate (Figure 4, N1) , the gate coupled to the second storage circuit (Figure 4, 34) so as to receive a value of the second bit (Figure 4, value of second bit BLB go to Q3 at node between Q3 and 34), and wherein the first storage circuit includes a flip flop (Figure 4, 33,34) that stores the first bit and that has a control node (Figure 4, N1) , the transistor further coupled between the control node and a fixed potential (Figure 4, Q3 coupled 34 and fixed potential VSS), and wherein the second storage circuit includes a flip flop that stores the second bit at a storage node (Figure 4, 31), the gate of the transistor being coupled to the storage node (Figure 4, Q4, coupled a node between Q4 and 34), and further including a bit line pair (Figure 4, BLB, XBLB) each coupled to one of the memory cells, each bit line pair coupled to logic that combines the respective bit line pair into a single logical value (Column 6, lines 64-67, Column 7, lines 41-51).

Allowable Subject Matter

6. Claims 4-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4-5 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Mukai (U.S. Patent No. 6,310,818), and others, does not teach the claimed invention having a first transistor having a source and drain coupled between the output enables of the first and second inverters and fixed potential, and gate coupled to the second storage circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

2/25/2006